Attorney Docket No. 0756-2203

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2815
Shunpei YAMAZAKI	)	Examiner: J. Jackson, Jr.
Serial No. 09/583,087	)	CERTIFICATE OF MAILING
Filed: February 1, 2000	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 19, 2005.
For: ELECTRO-OPTICAL DEVICE AND METHOD FOR MANUFACTURING THE SAME	)	Adalia M Stamper

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. 1.98(a).

An English Abstract of JP 54-154992 accompanied the Information Disclosure Statement filed November 2, 2001. A full English translation is submitted herewith. The Examiner is directed to page 4, lines 6-9 of the English translation.

JP 58-088787 was recently cited by the Japanese Patent Office against a counterpart Japanese application.

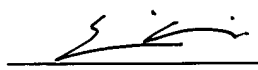
The remaining references were submitted to the Japanese Patent Office in connection with the features of "the analog switch" and "the CMOS transmission gate." In particular, the *Semiconductor Handbook, Basic Circuit of Analog Switch*, describes an analog switch circuit using the CMOS transmission gate shown in Fig. 11.65(d). The

analog switch circuit of Fig. 11.65(d) drives the switch consisting of Tr3 and Tr4, by providing a pair of gate pulses each of which has opposite polarity to the other. The pair of gate pulses are provided by inputting the gate input pulse to the inverter circuit consisting of Tr1 and Tr2. English translations of the drawings of the reference are shown on the copy of the reference by manuscript.

This Information Disclosure Statement is being submitted with an RCE. Therefore, no fee is required.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280. A duplicate copy of this sheet is attached.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/583,087
Filing Date	February 1, 2000
First Named Inventor	Shunpei YAMAZAKI
Group Art Unit	2815
Examiner Name	J. Jackson, Jr.
Attorney Docket Number	0756-2203

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	58-088787			05/26/1983		Full
		JP	54-154992			12/16/1979		Full
		JP	64-010711			01/13/1989		Abst.
		JP	01-236731			09/21/1989		Abst.
		JP	02-067819			03/07/1990		Abst.

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		H. YANAI, *3.3.2 Basic Circuit of Analog Switch,* Semiconductor Handbook, 2nd Edition, Pages 842-843, 1977.	Concise Statement

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.